CLAIMS

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1. A DMOS transistor for an IC circuit, comprising:

an epitaxial layer of a first conductivity type formed over a substrate;

a deep barrier region formed within adjoining surface portions of the substrate and the epitaxial layer;

a deep drain region extending from a surface of the epitaxial layer to outer peripheral regions of the deep barrier region to define a well region within the epitaxial layer;

a body region of a second conductivity type formed within the well region;

first and second source regions of the first conductivity type positioned at a surface of the well region and within the body region;

first and second portions of gate electrodes positioned above the first and second source regions, respectively, the body region, and the well region;

a conductive drain contact coupled to the deep drain region; and

a metallic source contact coupled to the first and second source regions and to a central portion of the well region.

2. The DMOS transistor of claim 1 wherein the metallic source contact and the central portion of the well region define a Schottky diode structure in parallel with an intrinsic body diode of the DMOS transistor.

3. The DMOS transistor of claim 2 wherein the Schottky diode replaces the intrinsic body diode of the DMOS transistor by diverting current from flowing through the intrinsic body diode.

4. The DMOS transistor of claim 1 wherein the resultant structure defines a Schottky diode which shunts a majority of current in recirculation avoiding a turn-on of parasitic devices.

5. The DMOS transistor of claim 2, further including a ring of the second conductivity type positioned in the central portion of the well region and in contact with the metallic source contact to increase a breakdown voltage of the Schottky diode.

6. A DMOS device for reducing the effects of parasitic devices in an IC circuit driving an inductive load, the device comprising:

an epitaxial layer formed on a substrate;

a well region formed by a deep drain region extending from a surface of the epitaxial layer and over a peripheral area of a deep barrier region located within the epitaxial layer and the substrate;

a body region within the well region, the body region containing first and second source regions;

a plurality of insulated gate electrodes formed over outer portions and inner central portions of the first and second source regions, respectively, the body region, and the well region;

a guard ring in a central surface portion of the well region and surrounded by the body region;

a first metallic contact coupled to the deep drain region; and

a Schottky metallic contact coupled to the source regions and to the central surface portion of the well region between the insulated gate electrodes and contacting the guard ring.

7. A DMOS device for reducing operational effects of parasitic devices associated with IC circuits, the device comprising:

a well region defined by a buried isolation region having an overlapping deep drain region within an epitaxial layer;

a body region containing first and second source regions within the well region;

insulated gates formed over a portion of the first and second source regions; and

a Schottky contact coupled to a central portion of the well region and spaced from the body region, the Schottky contact defining a portion of a Schottky diode within the epitaxial layer having operational characteristic means for reducing operational characteristics of parasitic devices associated with IC circuits.

8. The DMOS device of claim 7, further including a guard ring barrier spaced from the body region and adjacent to the Schottky contact, the guard ring barrier having operational characteristic means for increasing a breakdown voltage of the Schottky diode.

9. A DMOS transistor in an IC circuit, comprising:

an epitaxial layer of a first conductivity type formed over a substrate of a second conductivity type;

a drain region of a first conductivity type formed within the epitaxial layer;

a body region of the second conductivity type formed within the epitaxial layer;

a source region of the first conductivity type formed within the body region;

a gate electrode positioned above the source region, the body region, and the epitaxial layer;

a conductive drain contact coupled to the drain region; and

a metallic source contact coupled to the source region and to the epitaxial layer.

10. The DMOS transistor of claim 9 wherein the metallic source contact is in contact with the epitaxial layer at a surface of contact, the surface of contact forming a rectifying barrier.

11. The DMOS transistor of claim 10 wherein the surface of contact between the metallic source contact and the epitaxial layer forms a Schottky diode, the Schottky diode conducting current when a forward bias is applied from the metallic source contact to the conductive drain contact.

12. The DMOS transistor of claim 11 wherein the source region comprises two annular source regions separated by an annular region of the second conductivity type and the gate electrode comprises two annular gate electrodes positioned, respectively, above the two annular source regions; and

wherein the body region is an annular body region surrounding a central portion of the epitaxial layer, the central portion of the epitaxial layer being in contact with the metallic source contacts to form the Schottky diode.

13. The DMOS transistor of claim 12, further comprising:

a ring region of the second conductivity type formed in the central portion of the epitaxial layer, the ring region being in contact with the metallic source contact to increase a breakdown voltage of the Schottky diode;

a deep barrier region of the first conductivity type formed in the substrate below the epitaxial layer, the deep barrier region having a circular geometry with outer portions, the outer portions being in contact with the drain region.

14. A process for manufacturing a DMOS device in an IC circuit, the process comprising the steps of:

forming an epitaxial layer of a first conductivity type dopant over a substrate;

forming a deep barrier region within adjoining surface portions of the substrate and the epitaxial layer, the deep barrier region having a higher dopant concentration of the first conductivity type than the epitaxial layer;

implanting a deep drain region extending from a surface of the epitaxial layer to outer peripheral regions of the deep barrier region defining a well region within the epitaxial layer;

implanting a body region of a second conductivity type within the well region;

implanting first and second source regions of the first conductivity type at a surface of the well region and within the body region;

forming a first insulated gate above an outer portion of the first source region, the body region, and the well region;

implanting a guard ring in a central surface area of the well region and surrounded by the body region, the guard ring having a predetermined depth within the well region;

forming a second insulated gate above an inner central portion of the second source region, the body region, and the well region;

depositing a conductive drain contact over the deep drain region; and

depositing a conductive source contact over the first and second source regions and the central surface area of the well region inside the second insulated gate.

15. The process of claim 14, further including the step of implanting a central body region of the second conductivity type between the first and second source regions.

16. The process of claim 14, further including the step of implanting a deep isolation region of the second conductivity type extending from the surface of the epitaxial layer to the substrate, and circumferentially spaced from and surrounding the deep barrier region and the deep drain region.